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10/708,056	02/05/2004	Edmund M. Clarke	361007.000031	2055

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,056	CLARKE ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) *27-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26 and 33-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/15/04;3/6/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/708,056 and response to restriction requirement filed on 5/23/2006. Claims 1-3 and 33-46 is provisionally elected for examination with traverse. Claims 14-26 and 27-32 are withdrawn.

2. Applicants argued that the claims of Groups II (claims 14-26) and III (claims 27-32) recite features that are similar to the features recited in the claims of Group I. Examiner has partially agreed with Applicants. Examiner assert that Groups I and II recite similar feature. Therefore, Group I (claims 1-13 and 33-46) and II can be now be joint in the same group. However, Claims 27-32, in Group III, recite different features from those in Group I and II, now joint, are clearly independent and distinct inventions groups from Groups I and II. Although the claims can be classified in the same class and subclass, and the limitations as recited are different and distinct, the claim invention are independent and distinct. In addition, the claim limitations that are different and distinct require significant additional time for searching. Therefore, the inventions of Group II and combined Groups I & II are independent and distinct; and the restriction and restriction is proper made final.

Specification

3. The title of the invention is not descriptive because the invention refers to verifying behavioral consistency between two different language representations of description of a circuit design. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. Claim language in specification is vague when using "or the like) (For example [0016, 0018). Applicants are requested to use specific language.

Claim Objections

5. Claims 6-7 and 36 are objected to because of the following informalities: claim 6 should be dependent on claim 3 in order to properly define the claimed invention to thereby providing proper claim antecedent basis; claim 7 should be dependent on claim 6 in order to properly define the claimed invention to thereby providing proper claim antecedent basis. Claim 36 should be dependent on claim 34 in order to properly define the claimed invention. Examiner has examined the claims based on above suggestion. Appropriate correction is required.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 1-2, 5, 8-13; 14-26; 33-35, 37-38; 39-41 and 45-46 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The above claimed invention appears to be to an abstract idea than a practical application of the idea. The claimed invention does not result an output transformation that provides a useful, concrete and tangible result. For example, claim 1 clearly appears to be to an abstract idea than a practical application of the idea because two steps as recited provide no useful, concrete and tangible result. Claim 3 although

includes forming a first and second bit vector equations and comparing step, there is no indication of any output that is useful, concrete and tangible result. Accordingly, the claimed invention is appeared to be to an abstract idea because the claimed invention does not provide a practical application that produces a useful, concrete and tangible result. Applicant is remind that a tangible requirement does require that the claim must recite more than a 101 judicial exception to produce a real-world result. Therefore, since there is no real-world result, the claimed invention appears non-statutory.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 1, 33 and 39 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The steps as recited in claims 2 and 3 are considered to be critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). At least, Fig.1A shows that these steps must be recited in order to practice the claimed invention. Same rejection applies to claims 33 and 39.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 1, 14, 33 and 39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The recitation of applying a bounded model checking technique to a first and second computer languages of a circuit design is vague because one does not exactly know what it means by the recitation of applying. Claims needed to be specific. First computer language representation and second computer language representation need to be specific (applies to all independent claims). The same argument applies to limitation of determining a behavioral consistency between the two computer language representations. Determining a behavioral consistency (or not consistency) between the two computer languages needs to be specific as to what a behavioral consistency is referred to (claims 1, 11, 14, 16, 17, 24, 33, 39 and 43). Checking a satisfiability of the Boolean formula needs to be specific as what the Boolean formula is satisfiable (or satisfiable) is refereed to (claims 2, 8, 19, 21, 22, 34, and 41). Without precise claim language, it would cause claim construction problem because it lead to misinterpretation of the claim language. Note that the claimed invention is not broad but vague.

12. Claim 1, 33 and 39 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: the recitation of claims 2 and 3 because without these essential steps the claimed invention cannot be

practiced (see Fig. 1A). Note that without these essential steps the claims are vague, not broad.

13. All dependent claims, which are not specifically cited above, are also virtually rejected because of the deficiencies of their respective parent claims.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

15. Claims 1, 14, 33 and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Jain et al. (6,904,578 B2).

16. As to claims 1, 33 and 39 Jain et al. teach a method for verifying a property associated with a target circuit. The method comprising receiving information associated with a target circuit, the information identifying a property within the target circuit to be verified (see summary). The information of a target circuit comprises component, hardware, software (programs), object or element associated with digital processing of information or data (col. 3 lines 1-14; col. 5 lines 20-51). Jain et al. also teach algorithms that allow for a specific or designated property to be explored or

verified in target circuit (col. 5 lines 61-67), where the algorithms may include any suitable hardware, software, objects or elements operable to facilitate the verification operations being executed by POBDD data structure (col. 6 lines 2-11). Examiner has interpreted the recitation of information and algorithms including the programs or software as taught by Jain et al. to be a first computer language representation of a target circuit and a second computer language representation of a target circuit since the programs written describe behavior that is sought to be tested or verified in a target circuit. Jain et al. teach using or applying BMC tool to information received (referred to first and second computer language representation of the target circuit). Jain et al. further teach every propositional logic sentence needed to be checked or verified for equivalence in conjunctive normal form (col. 4 lines 23-43; col. 5 lines 20-51; col. 6 lines 1-67; col. 7 lines 1-36; col. 14 lines 4-22; col. 14 lines 37-57). This means that Jain et al. teach determining a behavioral consistency between the first and second computer language representations.

17. As to claim 14, Jain et al. teach a method for verifying a property associated with a target circuit. The method comprising receiving information associated with a target circuit, the information identifying a property within the target circuit to be verified (see summary). The information of a target circuit comprises component, hardware, software (programs), object or element associated with digital processing of information or data (col. 3 lines 1-14; col. 5 lines 20-51). Jain et al. also teach algorithms that allow for a specific or designated property to be explored or verified in target circuit (col. 5 lines 61-67), where the algorithms may include any suitable hardware, software, objects

or elements operable to facilitate the verification operations being executed by POBDD data structure (col. 6 lines 2-11). Examiner has interpreted the recitation of information and algorithms including the programs or software as taught by Jain et al. to be a first computer language representation of a target circuit and a second computer language representation of a target circuit since the programs written describe behavior that is sought to be tested or verified in a target circuit. Jain et al. teach using or applying BMC tool to information received (referred to first and second computer language representation of the target circuit). Jain et al. further teach every propositional logic sentence needed to be checked or verified for equivalence in conjunctive normal form (col. 5 lines 20-51; col. 6 lines 1-67; col. 7 lines 1-36; col. 14 lines 4-22; col. 14 lines 37-57). This means that Jain et al. teach determining a behavioral consistency between the first and second computer language representations. In addition, Jain et al. also teach that POBDD data structure 14 is an element operable to execute partitioning of BDD elements in a binary or digital environment. The POBDD data structure is a representation of a Boolean function for manipulation (col. 4 lines 24-64). Examiner has interpreted these teachings corresponding to unwinding a computer language representation of the circuit design and comparing the equations for consistencies. Further Jain et al. teach Boolean matching (read as comparing for consistencies between the first and second bit vector equations).

18. Claims 1-26 and 33-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Shtrichman (7,047,139 B2).

19. As to claims 1, 33 and 39, Shtrichman teaches substantially the same claim invention of a method to verify a circuit design comprising applying a bounded model checking technique to a first computer language representation of the circuit design and a second computer language representation of the circuit design and determining a behavioral consistency between the first and second computer language representations. Specifically, Shtrichman teaches a method of verification of the design of electronic devices using SAT-based bounded model checking (BMC) to identifying conflicts or derive conflict clauses (consistency/inconsistency between two computer language representations of a circuit design) by analyzing a set of formulas including a first formula relating to a first computer language representation of a circuit design and a second formula relating to a second computer language representation of the circuit design (summary, col. 8 lines 40-67 and col. 9-10 describe how SAT-based BMC tool is used to determine conflicts or consistency/inconsistency between a first formula and a second formula in sequence of SAT instances or BMC instances). The description of the electronic device can be written in hardware description languages (Verilog or VHDL). In addition, Shtrichman teaches certain languages or any languages are used in BMC and SAT solving (hardware description language) (col. 10 lines 66-67; col. 11 lines 1-26). Thus, Shtricchman teaches at least using two computer language representations of a circuit design.

20. As to claim 14, Shtrichman teaches substantially the same claim invention of a method for verifying a circuit design comprising applying a bounded model checking technique to a first computer language representation of the circuit design and a second

computer language representation of the circuit design and determining a behavioral consistency between the first and second computer language representations. Specifically, Shtrichman teaches a method of verification of the design of electronic devices using SAT-based bounded model checking (BMC) to identifying conflicts or derive conflict clauses (consistency/inconsistency) by analyzing a set of formulas (SAT formulas) including a first formula relating to a first computer language representation of a circuit design and a second formula relating to a second computer language representation of the circuit design (summary, col. 8 lines 40-67 and col. 9-10 describe how SAT-based BMC tool is used to determine conflicts or consistency/inconsistency between a first formula and a second formula in sequence of SAT instances or BMC instances). The description of the electronic device can be written in hardware description languages (Verilog or VHDL). In addition, Shtrichman teaches certain languages or any languages are used in BMC and SAT solving (hardware description language) (col. 10 lines 66-67; col. 11 lines 1-26). In addition, the first formula corresponds to a first bit vector equation and the second formula corresponds to a second bit vector equation, where the first and second computer language representations are unwounded.

21. As to claims 2, 18-19, 34-35 and 40, Shtrichman teaches SAT-based bounded model checking is used to solve representation associated with Binary Decision Diagrams (BDDs) or Boolean formula (col. 4 lines 19-67; col. 5 lines 1-26). In addition, Shtrichman teaches the clauses are formulated in a conjunctive normal form (CNF), and analyzing the second formula including forming a conjunction of the CNF of the second

formula with the identified conflict clauses and solving the conjunction. Further preferably, analyzing the first formula including determining while analyzing the first formula whether, for each of the conflict clauses, the clauses that lead to the respective conflict are in the subset of the clauses in the second formula (see summary, col. 6). At least these teachings correspond to jointly unwinding and checking a satisfiability of the Boolean formula.

22. As to claims 3, 36 and 42, remarks set forth in rejection claim 14 under Shtrichman equally apply because substantially same claim limitations.

23. As to claims 4 and 15, Shtrichman teaches a set of two or more SAT instances is defined for processing by a SAT-checking system corresponding to the claimed limitation translating each bit equation into a SAT instance (col. 5 lines 30-51).

24. As to claims 5, 20 and 41, Shtrichman teaches a method for satisfiability (SAT) testing, given a set of formulas describing a target system (description of circuit design) (col. 63-67, col. 6 lines 1-2).

25. As to claims 6 and 43, Shtrichman teaches using a SAT-based BMC to determining a consistency of the bit vector equations (first formula and second formula) (see summary; col. 9-10 describe determining conflict clauses).

26. As to claims 7, 16 and 44, Shtrichman teaches a process returns a counterexample corresponding to the solution, and the BMC analysis is complete (col. 10 lines 49-65).

27. As to claims 8, 17, 22 and 45, Shtrichman teaches a process for identifying conflict clauses that can be shared between SAT instances and solving a sequence of SAT instances in Fig. 3-4 (see col. 9-10 description).

28. As to claims 9, 23, Shtrichman teaches a verification processor finds an assignment of all of the variables in instance k that satisfied Sk, it means that the SAT problem has been solved. The process returns a counterexample corresponding to the solution and BMC analysis is complete. If no satisfiability assignment is found, the verification processor checks to determine whether instances should be checked, at a diameter checking step. Typically, the current value of k is checked against a predetermined diameter of the design, and if k has reached this diameter, the procedure terminated (a completeness threshold of a potential counterexample being exceeded) (col. 10 lines 49-65).

29. As to claims 10, 21 and 46, Shtrichman teaches the process returns a counterexample corresponding to the solution and the BMC analysis is complete (extracting a counterexample in response to the Boolean formula being satisfiable) (col. 10 lines 49-65).

30. As to claims 11, 24, Shtrichman teaches a process for verifying a circuit design using SAT-based BMC to determine conflict clauses (inconsistencies) described in Fig. 3-4 (see at least col. 9-10).

31. As to claims 12-13, 25-26, 37-38, Shtrichman teach a hardware description language (col. 8 lines 41-55; and certain languages or any language can be used (col.

10 lines 66-67; col. 11 lines 1-17). Since C type language is used to represent a circuit design, the languages as suggest must be included.

32. Claims 1-26 and 33-46 are rejected under 35 U.S.C. 102(a) as being anticipated by Clarke et al., "Hardware Verification using ANSI-C Programs as a Reference," DAC, Jan 03, pp. 308-311.

33. As to claims 1, 14, 33 and 39, Clarke et al. teach substantially the same claim invention of a verification of IC design method comprising applying SAT based Bounded Model Checking tool to a first and second computer language representations of the IC design and determining a behavioral consistency between the first and second computer language representations (page 308-310). The verification method comprises unwinding the first and second computer language representations of the IC design to form a first and second bit vector equations and comparing the first and second bit vector equations for consistencies (pages 309-311).

34. As to claims 2-13, 15-26, 33-38 and 40-46, Clarke et al. substantially teach the same claim limitations comprising jointly unwinding the first and second computer language representations to form a Boolean formula and checking a satisfiability of the Boolean formula, forming a first and second bit vector equations for comparing for consistencies (pages 308-311). The computer languages used include a hardware description language and C language as the claim invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

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